Sub E1 C2 Cont.

a third diffusion region which is formed between the second isolation region and the first diffusion region and near a surface of the semiconductor substrate and makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor; and

a silicide layer formed on a surface of the semiconductor substrate including the first and second isolation regions and a region connecting the first and third diffusion regions.

REMARKS

Claims 1-7, 20-23 and 25-26 are pending. By this Amendment, claims 1 and 20 are amended, and claims 8-19 and 24 are canceled. No new matter has been added. Reconsideration in view of the above amendments and following remarks is respectfully requested. The attached Appendix includes marked-up copies of each rewritten claim (37 C.F.R. §1.121(c)(1)(ii)).

I. INFORMATION DISCLOSURE STATEMENT

An Information Disclosure Statement with Form PTO-1449 was filed in the above-captioned patent application on May 30, 2001. Applications have not yet received from the Examiner a copy of the Form PTO-1449 initialed to acknowledge the fact that the Examiner has considered the disclosed information. The Examiner is requested to initial and return to the undersigned a copy of the Form PTO-1449. For the convenience of the Examiner, a copy of that form is attached.

II. THE CLAIMS DEFINE PATENTABLE SUBJECT MATTER

A. The Office Action rejects claims 1-4 and 25 under 35 U.S.C. §103(a) over U.S. Patent 6,268,639 (hereafter "Li '639") to Li et al. in view of either JP 406204475A to Natori or U.S. Patent 4,336,489 to Frederiksen and further in view of U.S. Patent 5,623,387 (hereafter "Li '387") to Li et al.; claim 5 under 35 U.S.C. §103(a) over Li '639, Natori and Li

'387 and further in view of JP 406224376A to Uchizumi et al.; claims 6-7 under 35 U.S.C. §103(a) over Li '639, Natori and Li '387 and further in view of U.S. Patent 5,949,094 to Amerasekera; and claims 20-23 and 26 under 35 U.S.C. §103(a) over Li '639 in view of Li '387 and either Frederiksen or Natori. Applicants respectfully traverse the rejections.

Li '639 fails to teach or suggest all of the features recited in independent claims 1 and 20. In particular, Li '639 fails to disclose semiconductor device including "a second isolation region formed between the MOS transistor and the first isolation region;...a second diffusion region which is formed in a region isolated by the second isolation region from the MOS transistor and makes up a lateral bipolar transistor together with a well in the semiconductor substrate and the first diffusion region of the MOS transistor; and a third diffusion region which is formed at a deeper position of the first diffusion region near the second isolation region and makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor" (emphasis added), as recited in claim 1, and similarly recited in claim 20.

The Office Action asserts that element 210 is a "second isolation region." See the Office Action at, e.g., page 4, lines 6-8. Applicants respectfully disagree with this assertion. Element 210 of Li '639 is a "p-diffusion" region through which a current will flow, not an isolation region. See Li '639, e.g., col. 4, lines 58-59 and col. 5, line 14. Even if, for argument sake, the Office Action intended to choose 120 "located most [to] the left" (as provided in the Office Action at page 11, lines 8-10), the n+ region 132 is located between the isolation region 120 and the far left isolation region 120, and is not formed in a region isolated by a second isolation region from a MOS transistor as recited in independent claims 1 and 20.

The Office Action also asserts that the "isolation region 210" is formed between the MOS transistors and the first isolation region. Applicants disagree with this assertion. Li

'639 specifically admits that a MOS transistor is not disclosed at col. 4, lines 26-30. Thus, Li '639 fails to teach or suggest the specific location of the CMOS relative to the first isolation region 210 (as defined in the Office Action). Therefore, one of ordinary skill in the art would not conclude that Li '639 provides the "second isolation region formed between the MOS transistor and the first isolation region."

Furthermore, the bipolar transistor in Fig. 2 of Li does not include the first diffusion region of the MOS transistor as recited in claims 1 and 20. In this connection, Li is silent about the first diffusion region of the MOS transistor partially making up the bipolar transistor and being isolated from the second diffusion region by the second isolation region, as recited in claims 1 and 20.

The Office Action refers to col. 2, line 50 and Fig. 2 and states that the element 132 is "a second diffusion region." It also asserts that the second diffusion region 132 is formed in a region isolated by the second isolation region (as previously defined as 210) and makes up a lateral bipolar transistor. Applicants respectfully disagree with this assertion. The P-diffusion region 210 is located deep within the substrate and is not located adjacent to the n+ region 132. Even if, for argument sake, it was possible to locate the p-diffusion region 210 adjacent to the n+ region 132, the p-diffusion region 210 would not isolate the n+ region 132. To the contrary, leakage would inherently result in this configuration, and to make such a modification would thwart the intended purpose of Li '639 to provide a protection circuit. Thus, Applicants submit that one of ordinary skill in the art would not have made this modification. Furthermore, the second diffusion region 132 of Li '639 is not isolated from a MOS transistor by the second isolation region (either 210 or 120, as disclosed in the Office Action). Instead, the second diffusion region 132 is isolated from the MOS transistor (as understood by the Office Action) by the first isolation region 120 (as defined by the Office Action).

The Office Action admits that Li '639 fails to teach or suggest a third diffusion region as recited in claims 1 and 20, and uses Frederiksen or Natori to compensate for this deficiency. However, neither Frederiksen or Natori cure the deficiencies of Li '639 noted above.

Instead, Frederiksen discloses that the Zener diode formed by elements 27 and 28 is created in an isolated region. See, e.g., the Abstract in col. 1, Lines 37-40. Accordingly, Frederiksen fails to disclose forming the Zener diode as a combination between the third diffusion region and a first diffusion region forming the MOS transistor. In addition, Frederiksen also fails to remedy the recognized deficiencies in Li '639, and does not provide any motivation, suggestion, or teaching to modify the disclosure of Li '639 to remedy these deficiencies.

Applicants respectfully request that before any further consideration of Natori, the PTO should provide a full translation of this Japanese reference. See Ex Parte Gavin, 62 USPQ2d 1680, Bd. Pat. App. & Inter. December 17, 2001. As understood from the Abstract of Natori, Natori also fails to compensate for the deficiencies of Li '387 stated above. In addition, Natori fails to teach or suggest providing a third diffusion region which is formed at a deeper position of a first diffusion region near the second isolation region and makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor. In fact, Natori fails to teach or suggest any first diffusion region near a second isolation region, and thus, fails to provide any motivation, suggestion, or teaching to modify the disclosure of Li '639. Natori fails to remedy the numerous deficiencies noted above with respect to Li '639.

The Office Action also correctly acknowledges that Li '639 fails to teach or suggest a second diffusion region that makes up a lateral bipolar transistor together with a well in the semiconductor substrate. The Office Action relies on Li ' 387 to compensate for this

deficiency. However, Li ' 387 also fails to compensate for the deficiencies of Li '639 noted above. Further, Uchizumi and Amerasekara also fail to compensate for the deficiencies of Li '639 noted above.

Accordingly, the Office Action has not established a prima facie case of obviousness, as the applied references fail to teach, suggest or render obvious all the subject matter of independent claims 1 and 20. Accordingly, the applied references also fail to render obvious the subject matter of claims 2-7, 21-23 and 25-26, which depend from independent claims 1 and 20 respectively. Withdrawal of the rejections under 35 U.S.C. §103(a) are therefore respectfully solicited.

III. CONCLUSION

In view of the foregoing, Applicants respectfully submit that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicants' undersigned representative at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Robert Z. Evora
Registration No. 47,356

JAO:RZE/dmw

Date: March 7, 2003

Attachment:
Appendix
Petition for Extension of Time
Copy of May 30, 2001 IDS, PTO-1449 and PTO date-stamped receipt

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APPENDIX

Changes to Claims:

Claims 8-19 and 24 are canceled.

The following is a marked-up version of the amended claims:

1. (Twice Amended) A semiconductor device comprising:

a semiconductor substrate;

a MOS transistor which is formed on the semiconductor substrate and includes a first diffusion region;

a first isolation region which isolates the MOS transistor from other MOS transistors on the semiconductor substrate;

a second isolation region formed between the MOS transistor and the first isolation region;

a silicide layer formed on a surface of the semiconductor substrate excluding the first and second isolation regions;

a second diffusion region which is formed in a region isolated by the second isolation region <u>from the MOS transistor</u> and makes up a lateral bipolar transistor together with a well in the semiconductor substrate <u>and the first diffusion region of the MOS transistor</u>; and

a third diffusion region which is formed at a deeper position of the first diffusion region near the second isolation region and makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor.

20. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a MOS transistor which is formed on the semiconductor substrate and includes a first diffusion region;

a first isolation region which isolates the MOS transistor from other MOS transistors on the semiconductor substrate;

a second isolation region formed between the MOS transistor and the first isolation region;

a second diffusion region which is formed in a region isolated by the second isolation region from the MOS transistor and makes up a lateral bipolar transistor together with a well in the semiconductor substrate and the first diffusion region of the MOS transistor;

a third diffusion region which is formed between the second isolation region and the first diffusion region and near a surface of the semiconductor substrate and makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor; and

a silicide layer formed on a surface of the semiconductor substrate including the first and second isolation regions and a region connecting the first and third diffusion regions.